

Day : Saturday
Date: 9/18/2004

Time: 21:35:00

PALM INTRANET

Continuity Information for 10/659954

Parent Data

10659954

is a continuation in part of 10455600.

Child Data

No Child Data

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- L1: (263484) isolation
- L2: (25502) 1 and gate.clm.
- L3: (10046) 2 and electrode.clm.
- L4: (3594) 3 and (capacitor and transistor)
- L5: (3558) 4 and (first or second or third)
- L6: (2373) 5 and (second near6 (gate or electrode)).clm.
- L7: (1462) 6 and (second near6 (region or area))
- L8: (434) 7 and (third near4 (gate or electrode)).clm.
- L9: (248) 8 and (capacitor.clm. or (lower adj. electrode).clm.)
- L10: (248) 8 and (capacitor.clm. or ((lower or bottom) adj elec
- L11: (196) 10 and (second near6 region).clm.
- L12: (152) 11 and ((first or second) near5 transistor)
- L14: (5) 13 and (different near3 thick\$4)
- L13: (159) 11 and thickness

Failed
 Saved

- (0) ("(thinadjfilm)nearresistor").PN.
- (0) ("(thinadjfilm)nearresistor").PN.
- (150130) thin adj film

New Edited Deleted Note Comment

2002-04-24 10:30:00

Author: SPATIUS-SPATIUS

Drafts

Highlighted terms only

12 and thickness

#	U	IPT #	Document ID	Issue Date	Pages	Title	Current CR	Current CR	Retrieval	Inventor	S	C	R	G	P	F
23	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020127811	20020912	438/300	Trench DRAM cell with vertical device and buried structure	438/300	257/300;		Noble, Wendell P.	<input checked="" type="checkbox"/>					
24	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020125336	20020912	257/368	SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURE	257/368	257/E21.65		Iwasa, Shoichi et al.	<input checked="" type="checkbox"/>					
25	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020123191	20020905	438/239	Method for fabricating a capacitor device with a conductive layer	438/239	257/E21.00		Huang, Chih-Mu et al.	<input checked="" type="checkbox"/>					
26	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020105089	20020808	257/774	Semiconductor device and manufacturing method	257/774	257/E21.50		Tanaka, Yoshinori	<input checked="" type="checkbox"/>					
27	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020096734	20020725	257/508	Semiconductor memory device and manufacturing method	257/508	257/903;		Natsume, Hidetaka	<input checked="" type="checkbox"/>					
28	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020066914	20020606	257/295	Ferroelectric memory and manufacturing method	257/295	257/E21.66		Imai, Keitaro et al.	<input checked="" type="checkbox"/>					
29	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020033494	20020321	257/295	Semiconductor memory device and method of fabrication	257/295	257/E21.66		Ozaki, Tohru et al.	<input checked="" type="checkbox"/>					
30	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020011616	20020131	257/295	Semiconductor device and method of manufacture	257/295	257/E21.57		Inoue, Kenichi et al.	<input checked="" type="checkbox"/>					
31	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020005534	20020117	257/296	Semiconductor memory device and method of manufacture	257/296	257/E21.01		Yamanaka, Toshiaki et al.	<input checked="" type="checkbox"/>					
32	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020000585	20020103	257/295	Semiconductor device having ferroelectric memory	257/295	257/E21.00		Ozaki, Tohru	<input checked="" type="checkbox"/>					
33	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020000583	20020103	257/257	System with meshed power and signal buses	438/238	257/E21.65		Kitsukawa, Goro et al.	<input checked="" type="checkbox"/>					
34	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20011220		TRENCH DRAM CELL WITH	438/238	257/E21.65		NOBLE, WENDELL P.	<input checked="" type="checkbox"/>						

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